TITLE

ABSTRACT OF THE DISCLOSURE

[0084] A parallel architecture for determining pixels inside a graphics primitive is provided. The architecture is a pipeline structure having a predetermined number of sequential logic circuits connected in series followed by a predetermined number of parallel logic circuits arranged in a pyramid structure. Each sequential logic circuit uses arithmetic edge functions corresponding to edges of a graphics primitive to determine whether a polygonal portion of a raster image is inside the graphics primitive. If the polygonal portion is at least partly inside the graphics primitive, the sequential logic circuit divides the polygonal portion into a predetermined number of subportions and computes descriptors (e.g., vertices and translated edge functions) for each subportion sequentially. Descriptors are then transferred sequentially to the next stage. Each parallel logic circuit performs the same functions as that of a sequential logic circuit except that a parallel logic circuit computes descriptors of the subportions in parallel and transfers them to the next stage in parallel.